

REMARKS

Claims 23-33 and 41-61 are pending in the subject application. Applicants' representative acknowledges with appreciation withdrawal of the 112, Second Paragraph, Rejection. Claims 23, 41-42, and 52-53 have been amended herein. Since the amendments place the application in condition for allowance, remove issues in the event of an appeal, and/or do not require further search, entry is respectfully requested. A listing of all claims is at pages 2-9. Favorable consideration in light of the amendments and the following remarks is respectfully requested.

The Anticipation Rejection

Claims 23-33 and 41-61 are rejected under 35 U.S.C. 102(a) over Moore (US 2001/0029152 A1). It is respectfully submitted that this rejection should be withdrawn for the following reasons. Independent claims 23, 41 and 52 (and dependent claims 42 and 53) have been amended herein to further clarify various aspects of the claimed invention and Moore fails to disclose such aspects. Pursuant to section 102, in order to establish anticipation, a single prior art document must disclose each and every element of a claim. Since Moore fails to disclose each and every element of the independent claims, Moore cannot anticipate claims 23-33 and 41-61.

Claim 23 recites **embedding** one or more electrical resistance members **within** a wafer, wherein resistance values of respective members are gathered and analyzed to facilitate determining wafer characteristics of a CMP process. Moore does not contemplate embedding one or more electrical resistance members within a wafer as recited in the subject claim. Rather, Moore discloses utilizing **a conductive layer** (layer 713) formed proximate (not embedded within) a substrate. This conductive layer is connected to an ohm meter, wherein resistance changes in the layer are detected and utilized to determine when planarization is complete and/or associated planarization parameters.

Proposed claim 41 recites **isolating a plurality** of electrical resistance members **within disparate layers** of a wafer and **coupling** such members to form an individual electrical resistance entity across the disparate layers, wherein a CMP process is controlled via an analysis of resistance information associated with the plurality of electrical resistance members. Moore is silent regarding employing a plurality of electrical resistance members, isolating such members, forming such members within disparate layers, and/or coupling such members to form a single entity. As described *supra*, Moore simply discloses utilizing a resistance measurement of a conductive layer proximate a substrate to determine when planarization is complete and/or associated planarization parameters.

Claim 52 recites forming at least a **first** and **second** electrical resistance members in **different directions within a layer** of a wafer, wherein these electrical resistance members are electrically **isolated** from each other and their respective resistances are utilized to characterize a CMP process. Moore does not disclose such aspects as described *supra*.

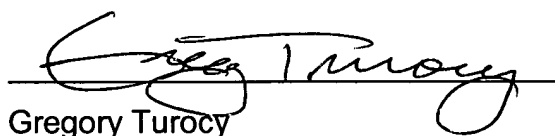
In view of the foregoing, it is readily apparent that Moore does not teach each and every element of claims 23-33 and 41-61. Accordingly, it is respectfully requested that this rejection be withdrawn.

Should the Examiner believe that a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact Applicants' undersigned attorney at the telephone number listed below.

In the event any fees are due in connection with the filing of this document, the Commissioner is authorized to charge those fees to our Deposit Account No. 50-1063.

Respectfully submitted,

AMIN & TUROCY, LLP

A handwritten signature in black ink, appearing to read "Greg Turocy", is written over a horizontal line.

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